

CLAIMS

Now, therefore, the following is claimed:

- 1 1. A processor purging system, comprising:
2 a translation lookaside buffer (TLB) having a plurality of translation pairs;
3 at least one memory cache; and
4 logic configured to detect whether at least one of the translation pairs
5 corresponds to a purge signal, the logic further configured to assert a purge detection
6 signal indicative of whether at least one translation pair corresponds to the purge
7 signal and to determine, based upon the purge detection signal, whether to search the
8 memory cache for a translation pair corresponding to the purge signal.

- 1 2. The system of claim 1, wherein the logic is further configured to purge the
2 translation pair from the memory cache if the translation pair corresponds to the purge
3 signal.

- 1 3. The system of claim 2, wherein the memory cache further comprises an
2 instruction queue.

- 1 4. The system of claim 3, wherein the memory cache further comprises a mini-
2 TLB.

1 5. The system of claim 2, further comprising compare logic configured to
2 compare the purge signal with each translation pair and assert a match signal
3 corresponding to each of the plurality of translation pairs if the purge signal
4 corresponds to one of the translation pairs, the logic further configured to deassert the
5 match signal corresponding to each of the plurality of translation pairs if the purge
6 signal does not match one of the translation pairs.

1 6. The system of claim 5, wherein the logic is further configured to collapse the
2 match signals corresponding to each of the plurality of translation pairs into the purge
3 detection signal indicative of whether at least one of the translation pairs corresponds
4 to the purge signal.

1 7. The system of claim 6, wherein the logic comprises a plurality of tiered logical
2 AND gates configured to collapse the plurality of signals into the signal indicative of
3 whether at least one of the translation pairs corresponds to the purge signal.

1 8. The system of claim 7, wherein the logic comprises a plurality of tiered logical
2 OR gates configured to collapse the plurality of signals into the signal indicative of
3 whether at least one of the translation pairs corresponds to the purge signal.

1 9. A computer readable medium having a program, the program comprising:
2 logic configured to detect whether at least one of a plurality of translation pairs
3 in a translation lookaside buffer (TLB) corresponds to a purge signal; and
4 logic configured to assert a purge detection signal indicative of whether at least
5 one of the translation pairs matched the purge signal.

1 10. The computer-readable medium of claim 9, wherein the program further
 2 comprises:
 3 logic configured to compare the purge signal with each translation pair of the
 4 TLB; and
 5 logic configured to assert a match signal for each translation pair of the TLB
 6 indicative of whether the translation pair corresponding to the matched signal matched
 7 the purge signal.

1 11. A processor purging system, comprising:
 2 a translation lookaside buffer (TLB) having a plurality of translation pairs;
 3 means for determining whether at least one of the translation pairs corresponds
 4 to a purge signal; and
 5 means for purging components of the processor based upon the determination
 6 of whether at least one of the translation pairs corresponds to a purge signal.

1 12. A method for purging a processor, comprising the steps of:
 2 detecting whether at least one of a plurality of translation pairs in a translation
 3 lookaside buffer (TLB) corresponds to a purge signal; and
 4 asserting a purge detection signal indicative of whether a translation pair
 5 matched the purge signal.

1 13. The method of claim 12, wherein the detecting step further comprises the steps
 2 of:
 3 comparing the purge signal with each translation pair of the TLB; and

4 asserting match signals for each translation pair of the TLB indicative of whether
5 the translation pair corresponds to the match signal.

1 14. The method of claim 13, wherein the asserting a purge detection signal step
2 further comprises the step of collapsing each match signal into a single purge detection
3 signal indicative of whether at least one of the translation pairs matched the purge
4 signal.

1 15. The method of claim 14, further comprising the step of deleting each translation
2 pair in the TLB that matches the purge signal.

1 16. The method of claim 15, further comprising purging processor components
2 resident on the processor if the purge detection signal indicates that at least one
3 translation pair in the TLB matches the purge signal.

1 17. A processor purging method, comprising:
2 detecting whether at least one translation pair in a plurality of translation pairs
3 within a translation lookaside buffer (TLB) corresponds to a purge signal;
4 asserting a purge detection signal indicative of whether at least one of the
5 translation pairs corresponds to the purge signal; and
6 determining, based upon the purge detection signal, whether to search the
7 memory cache for a translation pair corresponding to the purge signal.

1 18. A processor purging system, comprising:
2 a collection of translation pairs;
3 at least one memory cache;
4 means for asserting a purge detection signal indicative of whether at least one
5 translation pair corresponds to a purge signal; and
6 means for determining, based upon the purge detection signal, whether to search
7 the memory cache for the at least one translation pair corresponding to the purge signal.

1 19. A system for purging a processor, comprising:
2 a plurality of translation pairs;
3 means for detecting whether at least one of the plurality of translation pairs
4 corresponds to a purge signal; and
5 means for asserting a purge detection signal indicative of whether a translation
6 pair matched the purge signal.

1 20. The system of claim 19, further comprising means for determining, based upon
2 the purge detection signal, whether to search a memory cache for a translation pair
3 corresponding to the purge signal.